

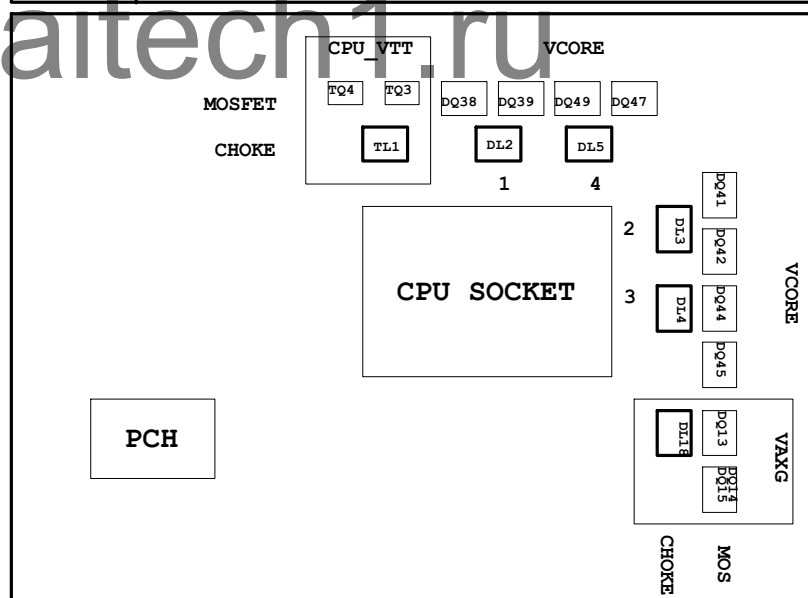
Model Name: GA-Z68AP-D3 2.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1155-A
05	CPU LGA1155-B
06	CPU LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH FDI,DMI,USB,PCIE
10	PCH DP,CLK BUFFER
11	PCH HOST,SATA,PCI
12	PCH GPIO,CTRL,AUDIO
13	PCH PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESSX4 SLOT / PCIE X1 SLOT
16	IT8892
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, LPT, TPM
20	Dual BIOS
21	ALC889
22	REAR AUDIO JACK
23	VCORE PWM ISL6364CRZ-1
24	VCORE PWM ISL6364CRZ-2
25	DISCRETE POWER
26	DDR 15V & VCC1 05 PCH PWM ISL6545CBZ
27	CPU VTT PWM ISL95870

SHEET TITLE

28	VCCSA POWER
29	F PANEL , F USB
30	ATX POWER, CLOCK GEN
31	HWM,KB/MS , FAN CTRL
32	REALTEK RTL8111E
33	ETRON 168A
34	HDMI
35	VAXG POWER, mSATA
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Gigabyte Technology			
Title	Cover Sheet		
Size	Document Number	GA-Z68AP-D3	Rev
Custom			2.0
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GA-Z68AP-D3

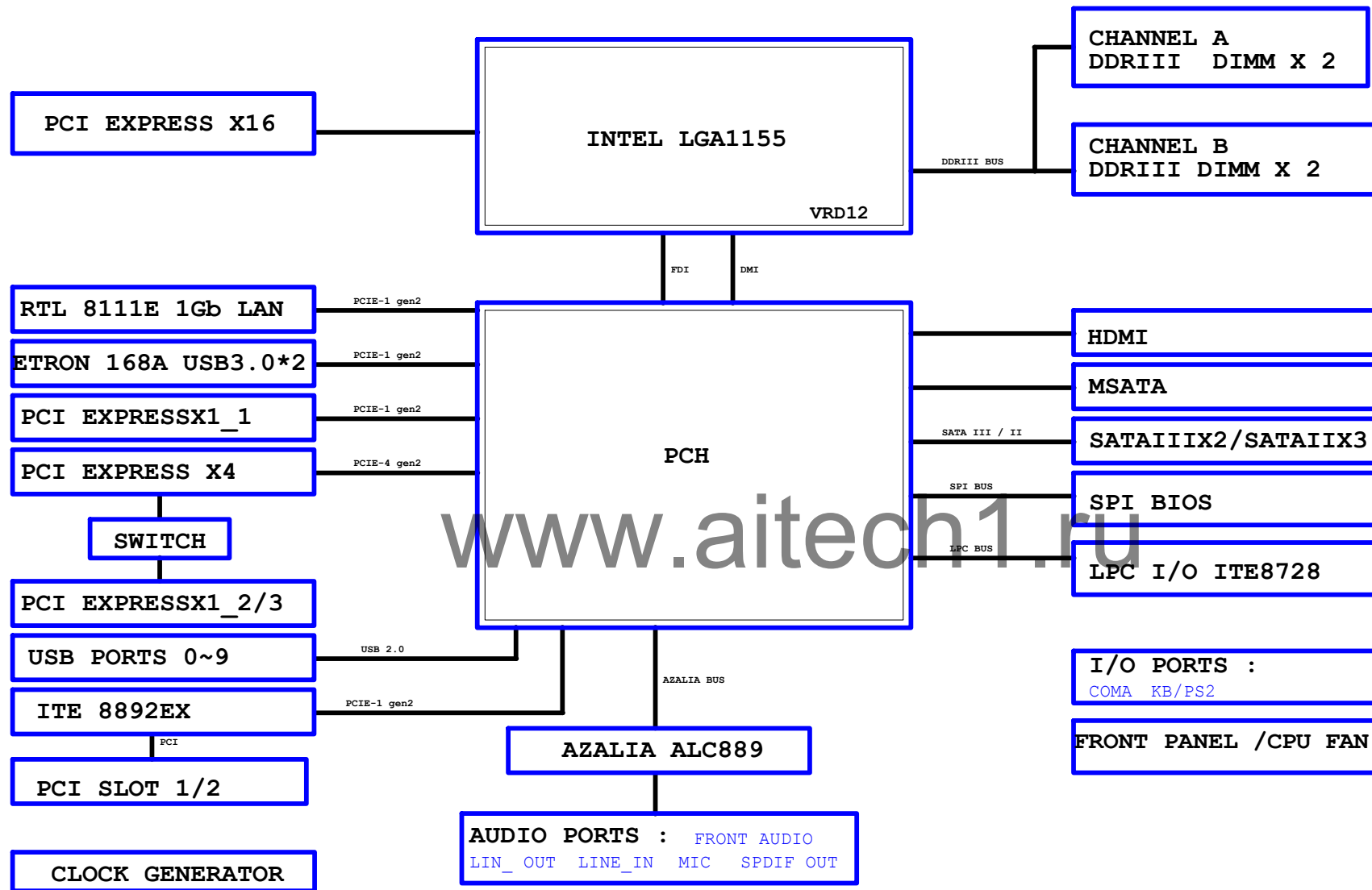
Component value change history

[illegible]

Circuit or PCB layout change

DATE	Change Item	Reason
2010/07/05 PCB:0.1	1.NEW MODEL: P67A-D3-0.1	
2010/08/18 PCB:0.2	由GA-P67A-D3-0.1 rename GA-P67A-UD3-0.2	
	1.update MOS_HS footprint 2.20z copper pcb	
2010/10/05 PCB:0.1	由GA-P67A-UD3-0.2 修改	
2010/10/18 PCB:0.2	1.確認SATA 6GB PORT0 OR PORT1???	
	2.NO TURBO USB3.0 ,SUR1~SUR8 ----->SHORT WIRE	
2011/01/10 PCB:0.2	1.NEW MODEL: P67A-D3-0.2 由 P65A-D3-0.2修改	
	1.co-layer 電容移除	
	2.CPU VCORE 電容多留不用的MASK起來	
	3.0 OHM----->SHORT-WIRE	
2011/02/08 PCB:0.1	由0.2修改----->RENAME GA-P67A-D3-B3	
	1.co-layer 電容移除	
	2.CPU VCORE EC14,DEC4,DEC5,DEC6,TEC8電容移除;調整MOS_HS與CHOKES及電容的位置避免撞件	
	3.PCH VCC1_05 switch power----->linear power	
2011/02/24 PCB:1.0	1.CR49,CR50 short-wire ----->open,add LR15 FOR AUDIO line out SNR issue	
	2.DR290,DR293,DR312,DR333,DR351,R264,CR31 0 OHM----->SHORT-WIRE	
	3.背面電容mask	
	4.ADD TBC40,TBC41 to reduce CPU VTT power ripple	
2011/03/30 PCB:1.0T	1.ADD CLOCK BUFFER	
2011/05/04 PCB:0.1	1.由P67A-D3-B3-1.0T修改	
	2.DEL CLOCK GEN.	
	3.ADD HDMI, mSATA ,CPU VAXG POWER	
2011/05/15 PCB:1.0	1.Z68AP-D3-1.0 FOR MP	
2011/06/23 PCB:0.1	1.GA-Z68AP-S3由Z68AP-D3-1.0修改	
	2.CPU VCORE / VTT 上1下1,DDR TO-252 MOS,ALL IRON CHOKES.	
	3.NO 3X 力,單一POLY FUSE,NO SMART FAN; pure mSATA	
2011/08/04 PCB:2.0T	1.GA-Z68AP-S3-0.1 RENAME GA-Z68P-DS3-2.0T----->RENAME Z68AP-D3-2.0T	
	2.ADD ITE8275 FOR DES,ALC889,全日固	
2011/09/15 PCB:2.0	1.RENAME Z68AP-D3-2.0T -----> 2.0 for MP	

BLOCK DIAGRAM



LGA1155A

MAAA0 AV27
MAAA1 AV24
MAAA2 AW24
MAAA3 AW23
MAAA4 AV23
MAAA5 AV23
MAAA6 AT24
MAAA7 AU22
MAAA8 AV22
MAAA9 AT22
MAAA10 AV28
MAAA11 AU21
MAAA12 AT21
MAAA13 AW32
MAAA14 AU20
MAAA15 AT20

7 -SWEA <- -SWEA AV29
7 -SCASA <- -SCASA AV30
7 -SRASA <- -SRASA AU28
7 SBAA0 <- SBAA0 AY29
7 SBAA1 <- SBAA1 AW28
7 SBAA2 <- SBAA2 AV20
7 -CSA0 <- -CSA0 AU29
7 -CSA1 <- -CSA1 AV32
7 -CSA2 <- -CSA2 AW30
7 -CSA3 <- -CSA3 AU33

7 CKEA0 <- CKEA0 AV19
7 CKEA1 <- CKEA1 AT19
7 CKEA2 <- CKEA2 AU18
7 CKEA3 <- CKEA3 AV18
MODT_A0 AV31
MODT_A1 AU32
MODT_A2 AU30
MODT_A3 AW33

7 DCLKA0 <- DCLKA0 AY25
7 -DCLKA0 <- -DCLKA0 AW25
7 -DCLKA1 <- -DCLKA1 AU24
7 -DCLKA1 <- -DCLKA1 AU25
7 -DCLKA2 <- -DCLKA2 AW27
7 -DCLKA2 <- -DCLKA2 AY27
7 DCLKA3 <- DCLKA3 AV26
7 -DCLKA3 <- -DCLKA3 AW26

7,8 -DDR3_RST <- TR1
0.1u4/4X7R/16V/K/X
TBC9
0.1u4/4X7R/16V/K/X

AV13
AV12
AU12
AU14
AU13
AU13
AU13
AU11
AU12
AU12

DDR_0

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CPU-SK/1155/S/15

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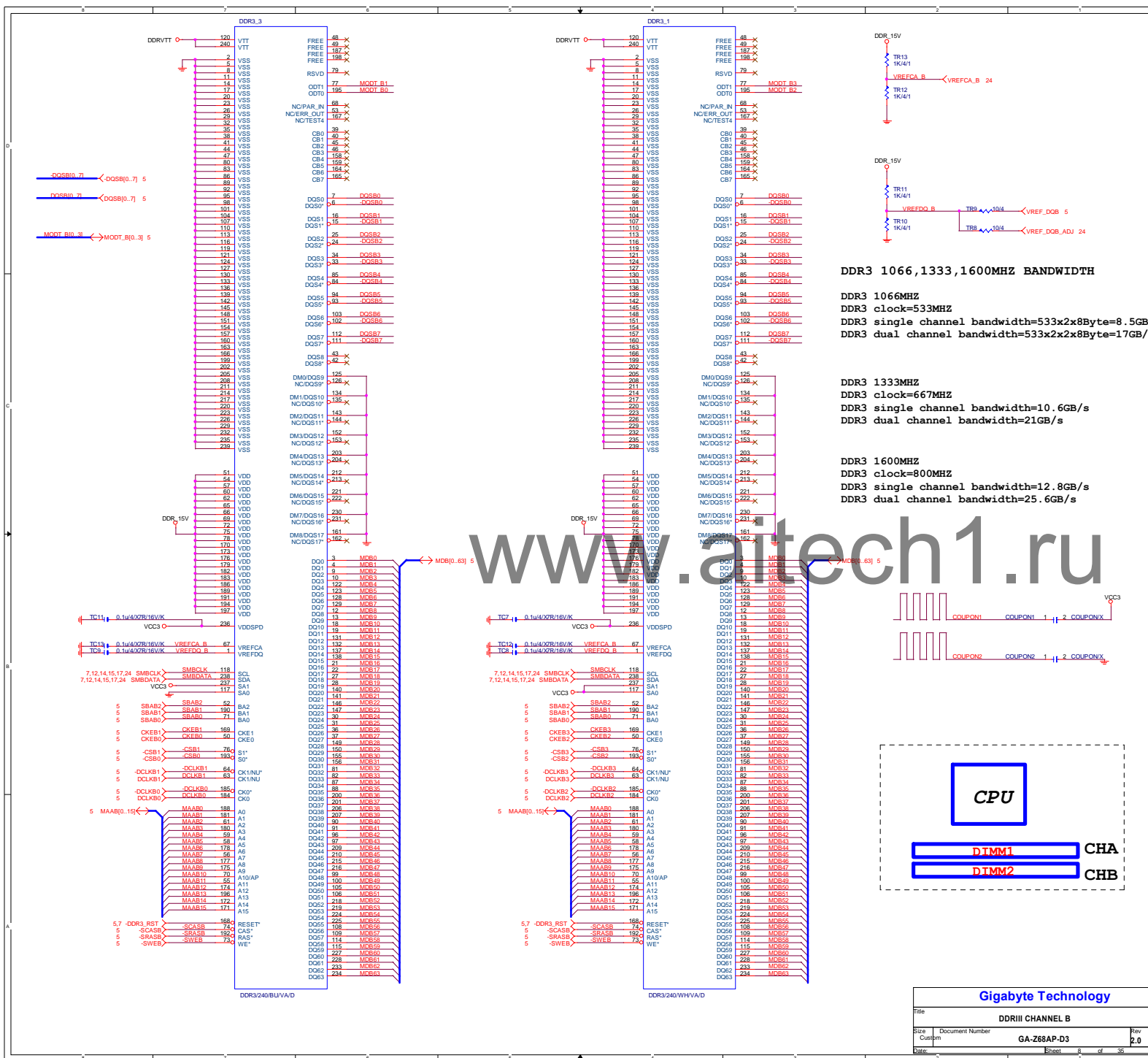
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SATA:20/4.5/7.5/4.5/20 (breakout min 8/4/4/8)
Impedance=90 +- 17.5%

PCHC

PCHA

PCHB

PCHD

PCH5

PCH6

PCH7

PCH8

PCH9

PCH10

PCH11

PCH12

PCH13

PCH14

PCH15

PCH16

PCH17

PCH18

PCH19

PCH20

PCH21

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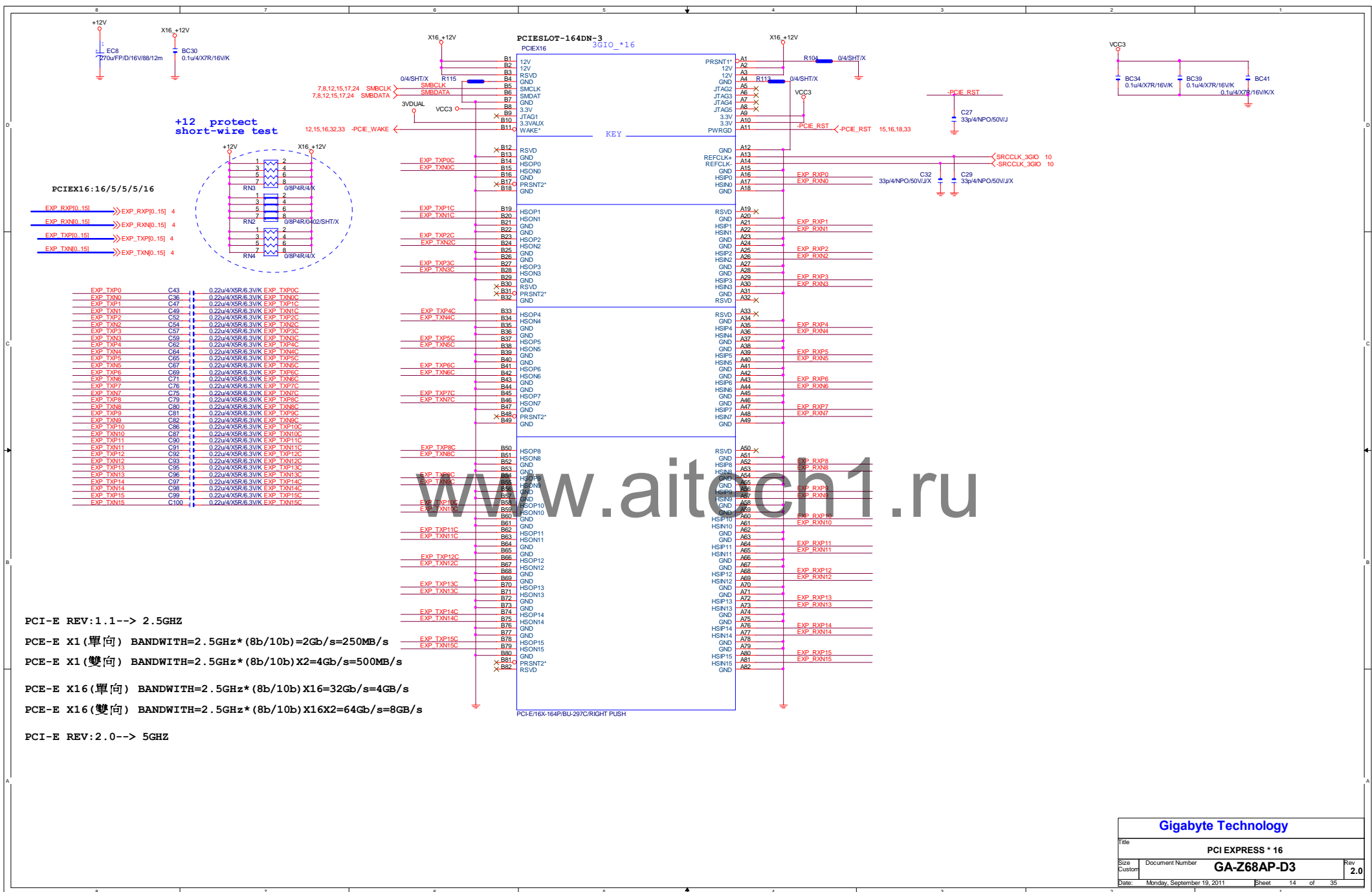
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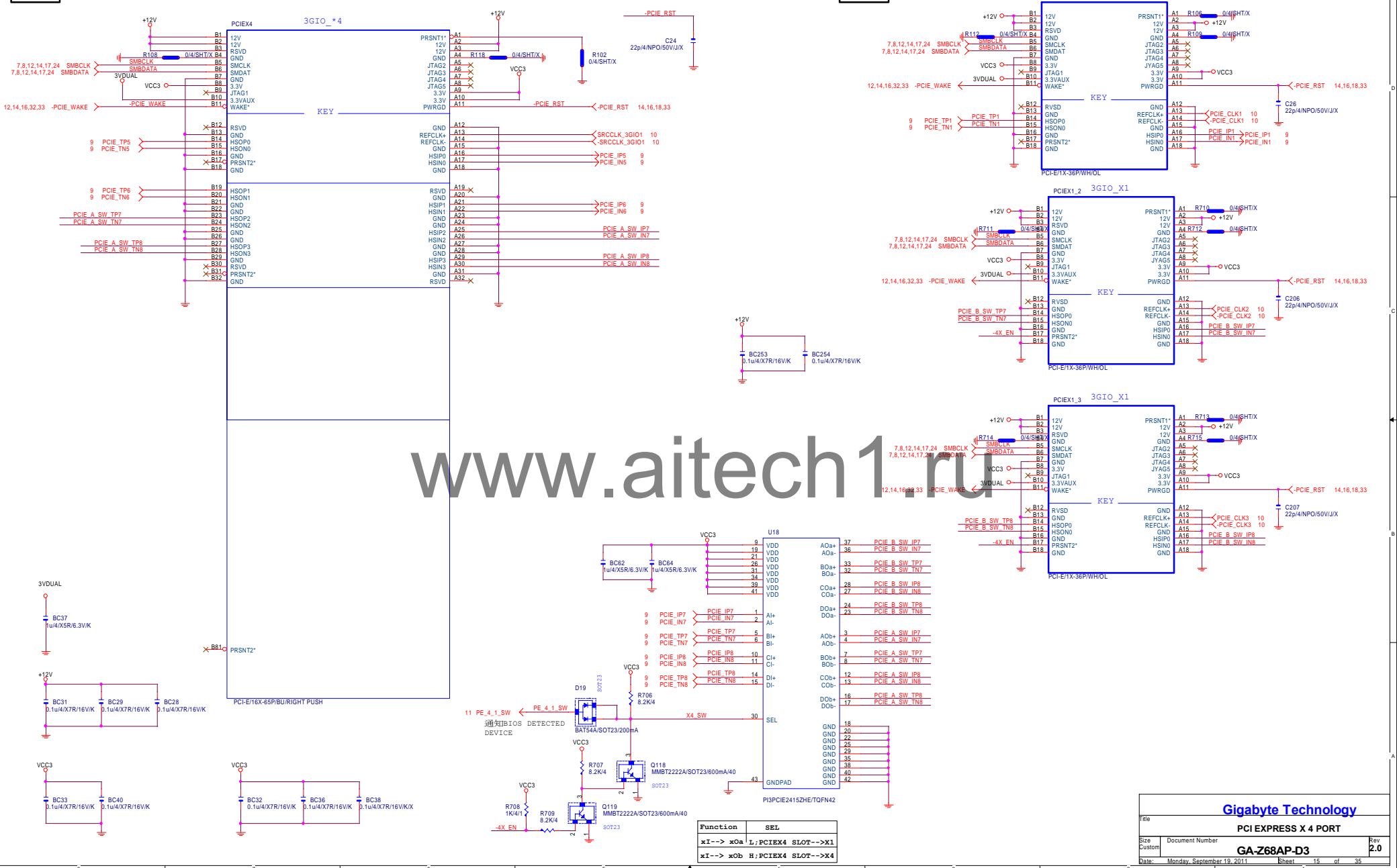
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PCIE*4

PCIE*1

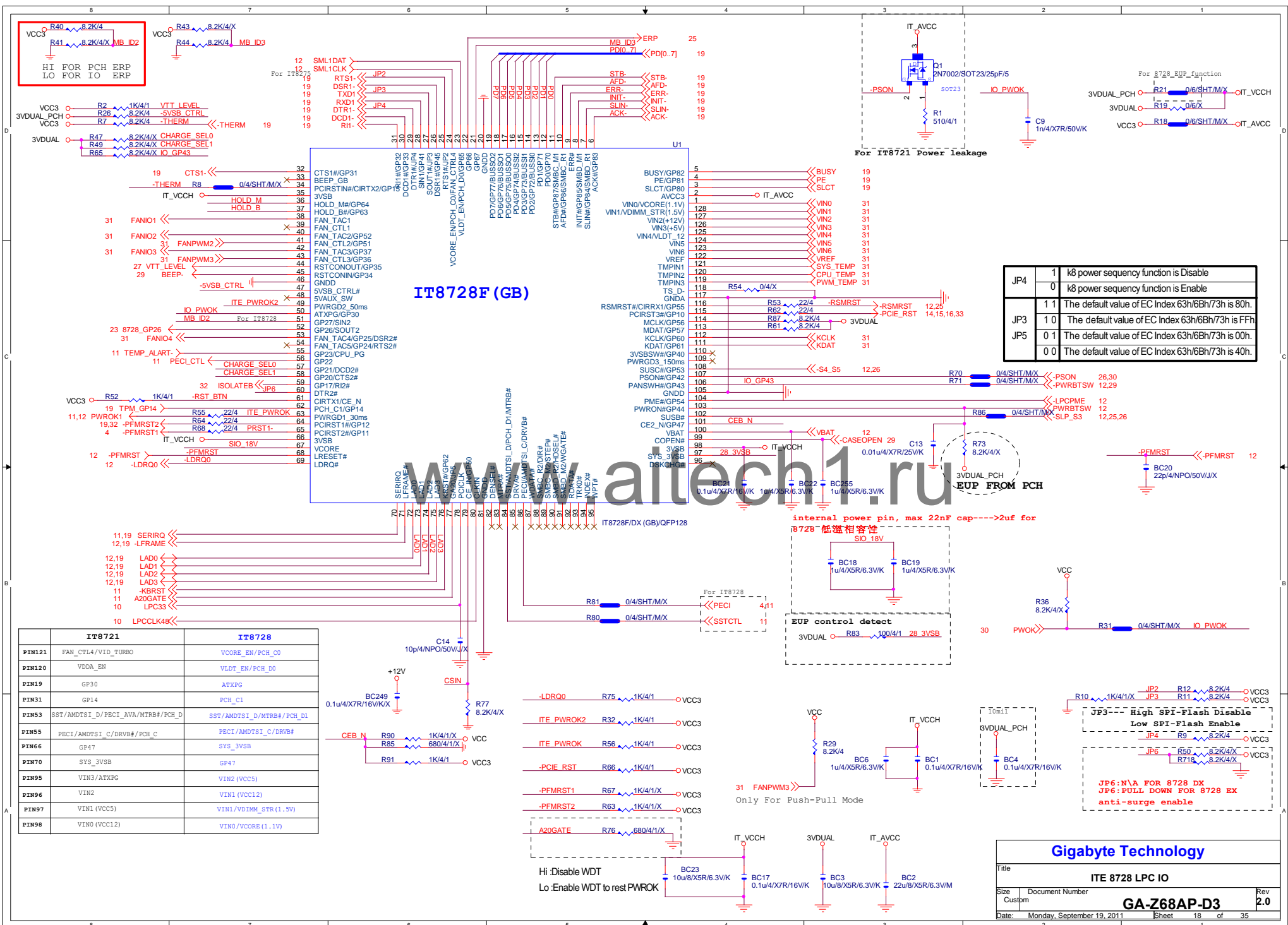


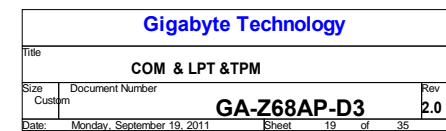
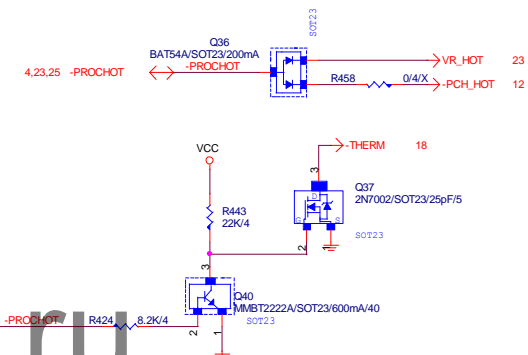
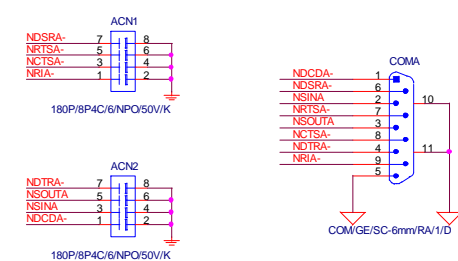
Gigabyte Technology

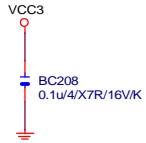
File: **PCI EXPRESS X 4 PORT**

Size: **Custom** | Document Number: **GA-Z68AP-D3** | Rev: **2.0**

Date: **Monday, September 19, 2011** | Sheet: **15** of **35**

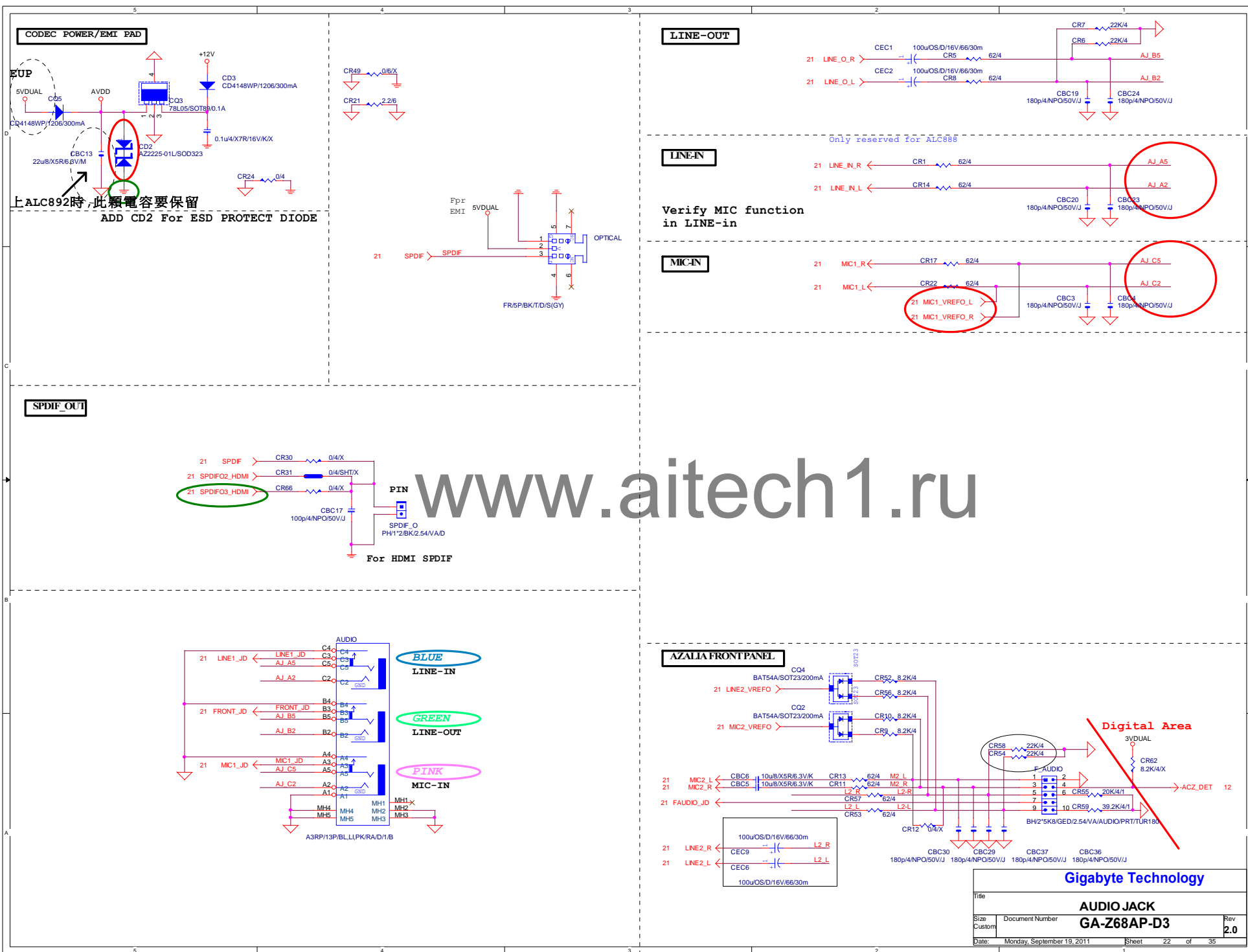


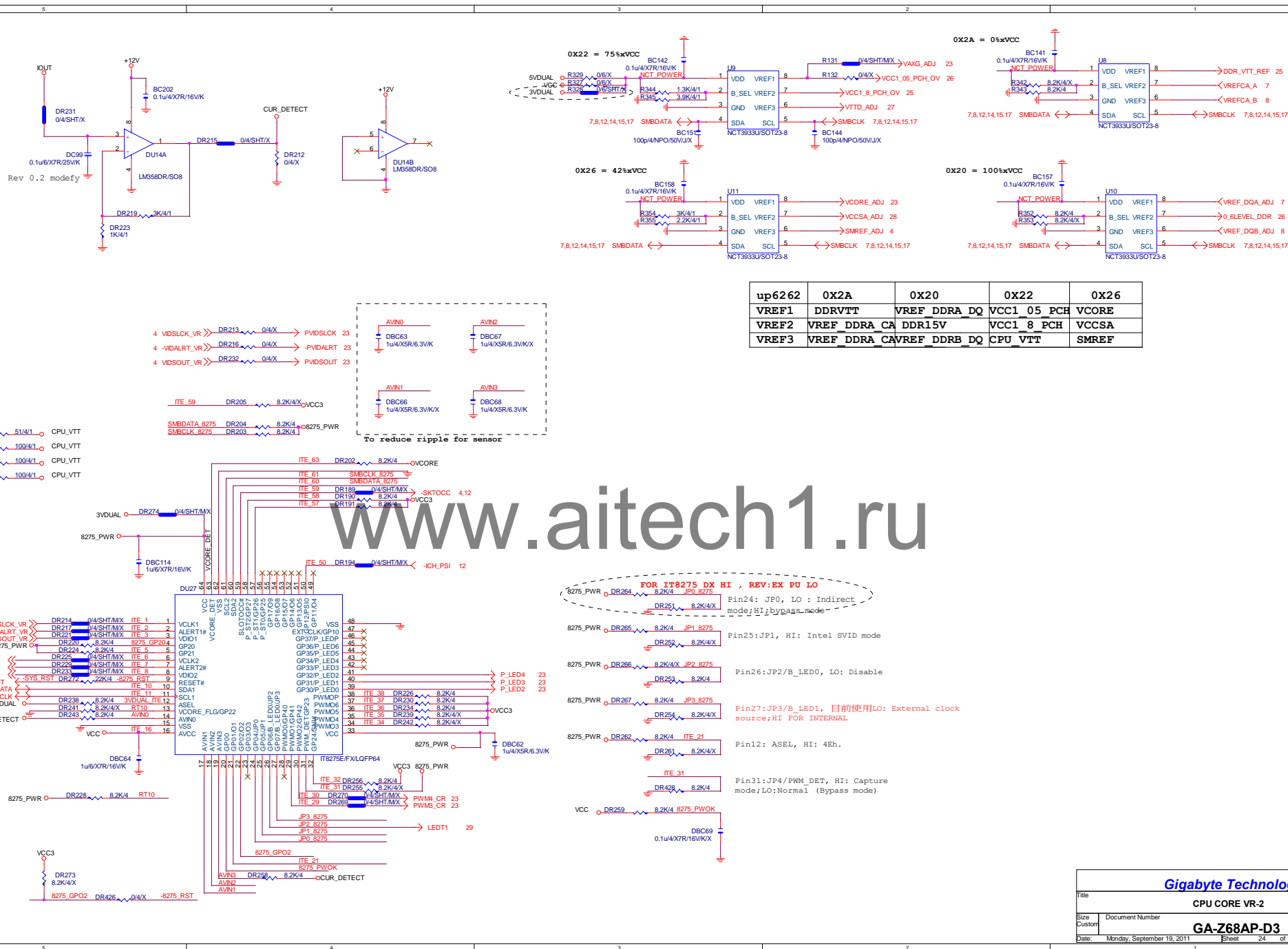


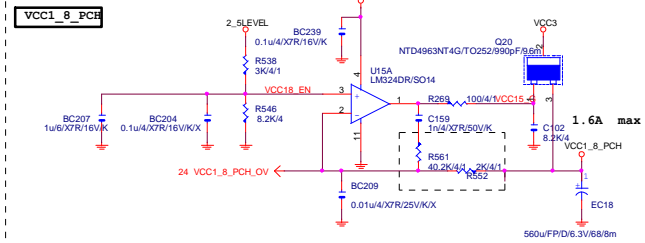


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Gigabyte Technology			
Title		BIOS	
Size	Document Number	GA-Z68AP-D3	
Custom			Rev 2.0
Date: Monday, September 19, 2011		Sheet 20 of 35	







The schematic diagram shows the RT9173DPS3/S0B/S regulator circuit. The input is a 15V DDR supply connected to the VIN pin (pin 1) of the U13 regulator. A 1μF/4.7V capacitor (C199) is connected between the input and ground. The GND pin (pin 2) is connected to ground. The VREF1 pin (pin 3) is connected to a 1k/4.7V resistor (R508) which is connected to the 15V supply. The VOUT pin (pin 4) is connected to the 5V DUAL VCC output. A 10μF/8.3V capacitor (C137) is connected between the output and ground. The VREF2 pin (pin 7) is connected to the 5V DUAL VCC output. The VENABLE pin (pin 8) is connected to the 5V DUAL VCC output. The VCNTRL pin (pin 6) is connected to ground. The BOOT_SEL pin (pin 5) is connected to ground. The 5V DUAL VCC output is also connected to a 1k/4.7V resistor (R505) which is connected to ground. A 1A max current limit is indicated on the output line.

FOR PCH ERP

5VSB

R578 22K/4

R577 8.2K/4

5V_L_EN

C163 0.1uF/4X7R/16V/K

D73 PMBT2907A/SOT23-600mA/50

R579 220/6

5V_L

5VSB

D75 PMBT2907A/SOT23-600mA/50

R580 220/6

R581 220/6

12V

RS2 CLOSE CPU VR MOSFET

deasserted at 116 degree

PROCHOT → PROCHOT 4.1923

Q54
2N7002/SOT23/25pF5

SOT23

U15C
LM324DR/SO14

TSM 5

TSM 6

R404
10K/1

R418
6K/4/1

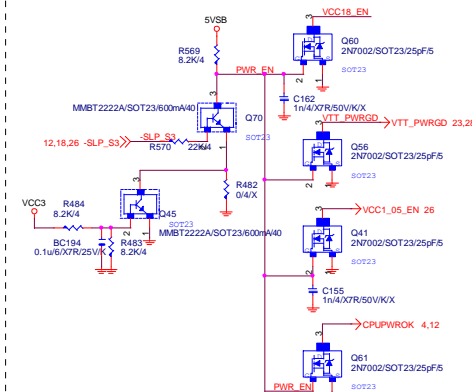
R425
10K/1

R426
1K/1

C175
0.1u/4X7R/16V/KX

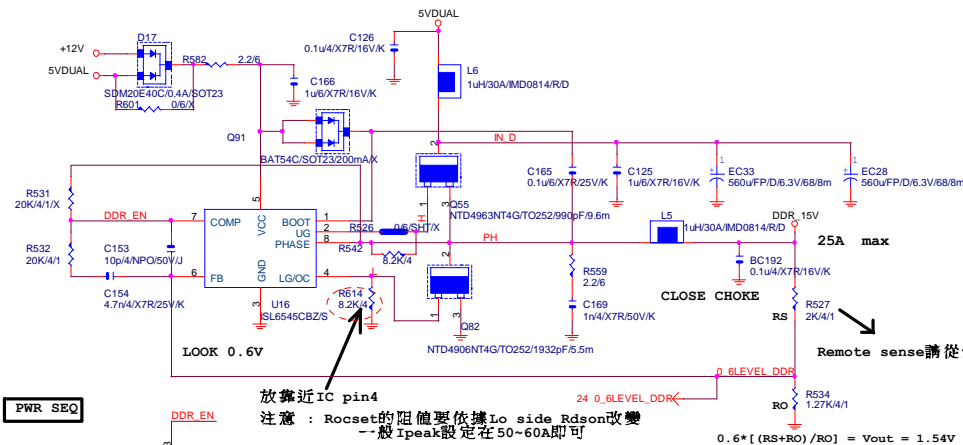
C176
100nF/50V/KX

CLOSE PWM HOT MOSFET



Title			
DISCRETE POWER			
Size	Document Number		Rev
C	GA-Z68AP-D3		2.0
Date:	Monday, September 19, 2011	Sheet	25 of 35

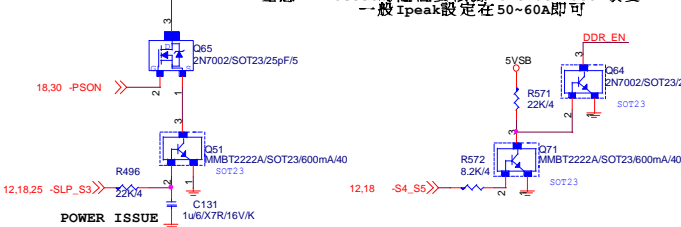
DDR18V



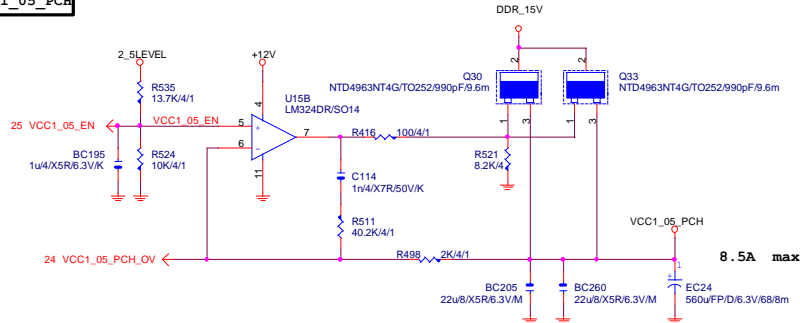
VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
IRMS=11.45A
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7 (85°C), 1 (105°C)
VIN Ripple current=4.7X1.7=7.99A (85°C)
-->故固態電容須2X7.99=15.98>11.45A

OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
typ $I_{ocset} = 20\mu A$, $R_{ocset} = 4.7k$
OCP : $53.71A = (2 \times 20\mu A \times 4.7k) / (7m / 7m)$

PWR SEQ



VCC1_05_PCH



VIN=3.3V, VOUT=1.05V, IOUT=8.5A, PHASE=1
IRMS=3.959A
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7 (85°C), 1 (105°C)
VIN Ripple current=4.7X1.7=7.99A (85°C)
-->故固態電容須2X7.99=15.98>11.45A

OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
typ $I_{ocset} = 20\mu A$, $R_{ocset} = 8.2k$
OCP : $46.86A = (2 \times 20\mu A \times 8.2k) / 7m$

Gigabyte Technology			
Title	DDR_15V		
Size	Custom	Document Number	GA-Z68AP-D3
Date	Monday, September 19, 2011	Sheet	26 of 35
Rev	2.0		

The image displays a detailed PCB layout for an ATX power connector. The central feature is the ATX connector footprint, a 24-pin D-sub connector, with pins numbered 1 through 24. The layout includes the following components and connections:

- Power Rails:**
 - +12V:** Connected to pins 1, 2, 11, and 12. A 5VSB (Standby) pin (pin 9) is also connected to +12V.
 - +5V:** Connected to pins 4, 5, 14, and 15.
 - +3.3V:** Connected to pins 13, 16, 17, and 18.
 - 12V:** Connected to pin 20.
 - 5V:** Connected to pin 21.
 - GND:** Connected to pins 3, 6, 7, 8, 9, 10, 19, 22, 23, and 24.
- Control Signals:**
 - PS-ON:** Connected to pin 16.
 - POK:** Connected to pin 20.
- Protection Components:**
 - BC214, BC215, BC227:** 2N2222 PNP transistors used for level shifting or protection on the +12V line.
 - BC218, BC219, BC220, BC221, BC222, BC223, BC224:** 2N2222 PNP transistors used for level shifting or protection on the +5V and +3.3V lines.
 - BC225:** 2N2222 PNP transistor used for level shifting or protection on the -12V line.
 - BC216, BC217, BC221, BC222, BC223, BC224, BC225:** 0.1uF/50V electrolytic capacitors used for decoupling.
- Other Components:**
 - AD1:** A 1N4148 diode used for protection on the +12V line.
 - APW1212IV/VA/SN2SHKPA66:** A 12V/1.2A DC-DC converter used for the +12V output.
- Mechanical Features:**
 - HOLE_3X:** Three circular holes for mounting the connector.
 - Dimensions:** The layout includes various dimensions for the connector footprint, including a 1.27mm pitch for the pins and a 1.27mm diameter for the mounting holes.

The layout is titled "ATX POWER CONNECTOR" and includes a revision history table at the bottom right.

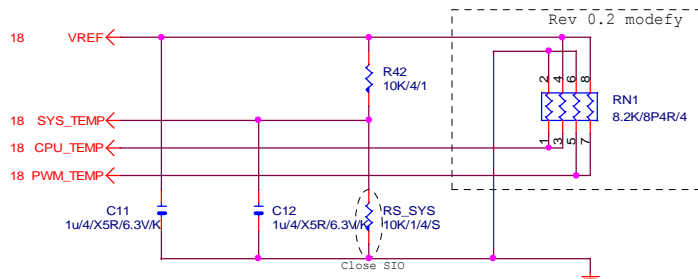
Rev	Description	Date
1.0	Initial Release	2011-09-19
2.0	Revise the connector pin assignment	2011-09-19

The image displays a detailed PCB layout for an ATX power connector. The central feature is the ATX connector footprint, a 24-pin D-sub connector, with pins numbered 1 through 24. The layout includes the following components and connections:

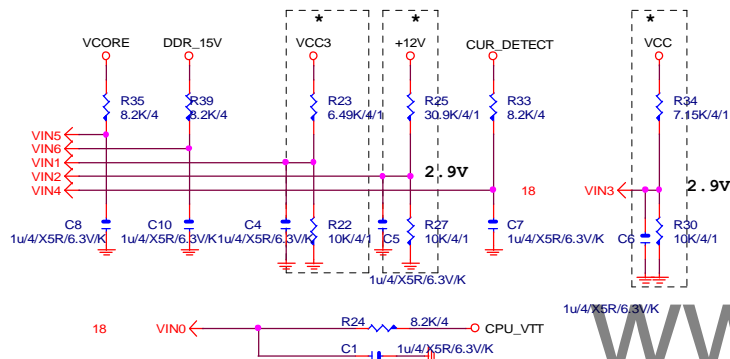
- Power Rails:**
 - +12V:** Connected to pins 1, 2, 11, and 12. A 5VSB (Standby) pin (pin 9) is also connected to +12V.
 - +5V:** Connected to pins 4, 5, 14, and 15.
 - +3.3V:** Connected to pins 13, 16, 17, and 18.
 - 12V:** Connected to pin 20.
 - 5V:** Connected to pin 21.
 - GND:** Connected to pins 3, 6, 7, 8, 9, 10, 19, 22, 23, and 24.
- Control Signals:**
 - PS-ON:** Connected to pin 16.
 - POK:** Connected to pin 20.
- Protection Components:**
 - BC214, BC215, BC227:** 2N2222 PNP transistors used for level shifting or protection on the +12V, +5V, and -12V lines.
 - BC218, BC219, BC220, BC221, BC222, BC223, BC224:** 1N4148 diodes used for protection or signal conditioning.
 - BC225:** A 1N4148 diode used for protection on the PS-ON line.
- Other Components:**
 - AD1:** A 1N4148 diode used for protection on the +12V line.
 - APW1212IV/VA/SN2SHKPA66:** A 12V, 1.2A, 1W, 1% tolerance resistor used for current sensing or protection.
- Mechanical Features:**
 - HOLE_3X:** Three circular holes for mounting the connector.
 - Dimensions:** The layout includes various dimensions for the connector footprint and the overall board size.

The layout is titled "ATX POWER CONNECTOR" and is part of a larger project, as indicated by the "GA-Z68AP-D3" label in the bottom right corner.

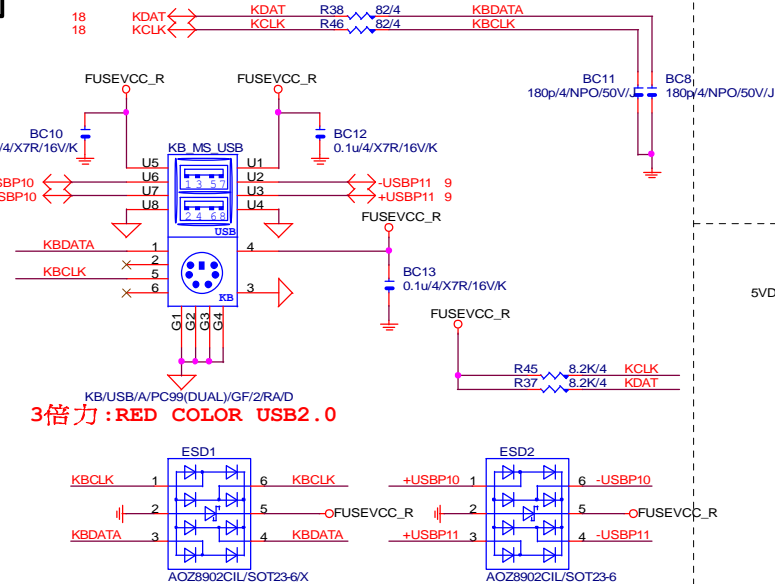
TEMP H/W MONITOR



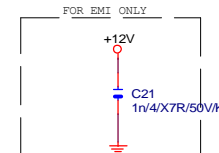
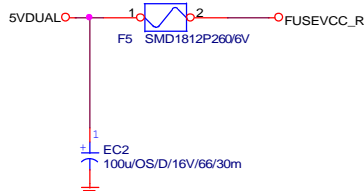
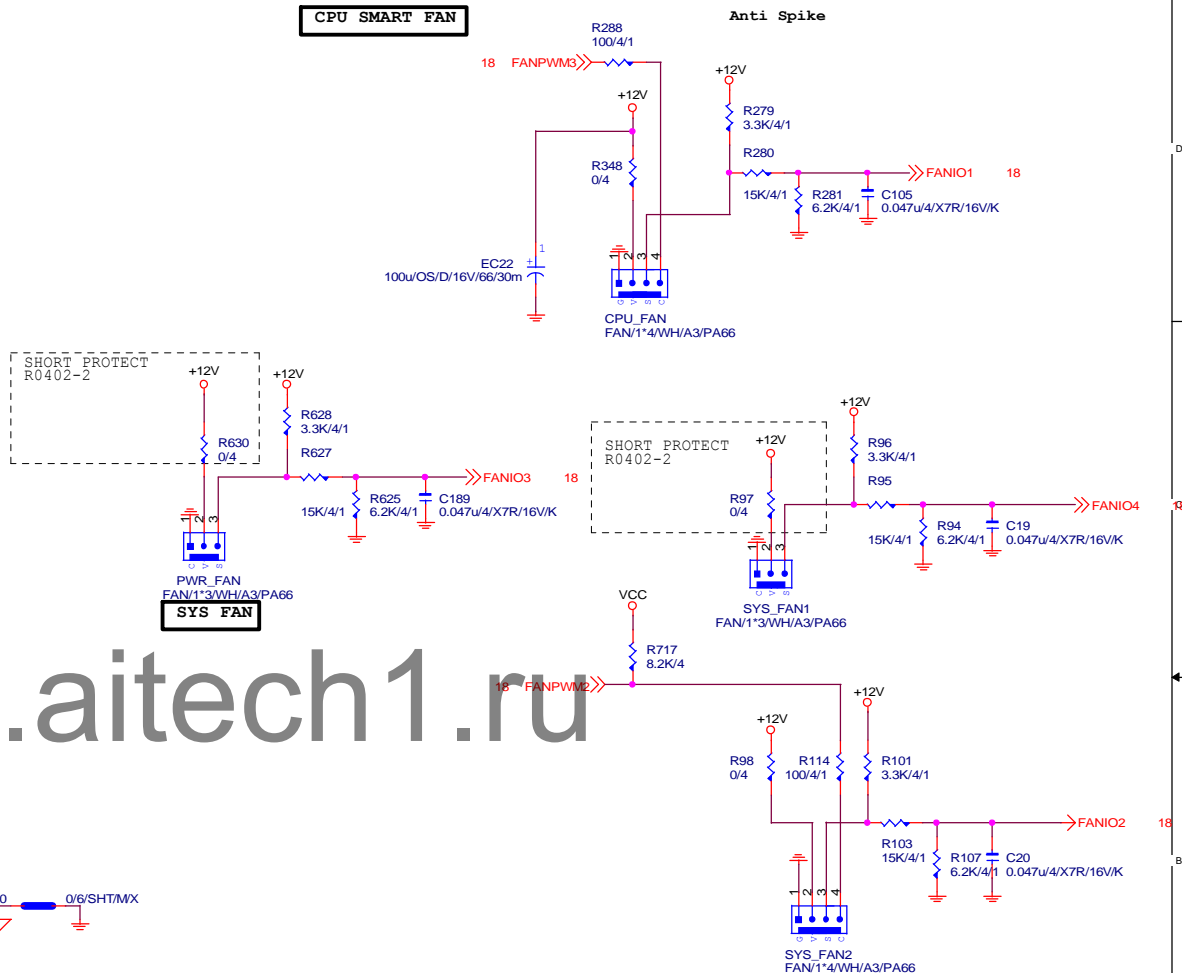
VOLTAGE-- H/W MONITOR



KB/USB



CPU SMART FAN



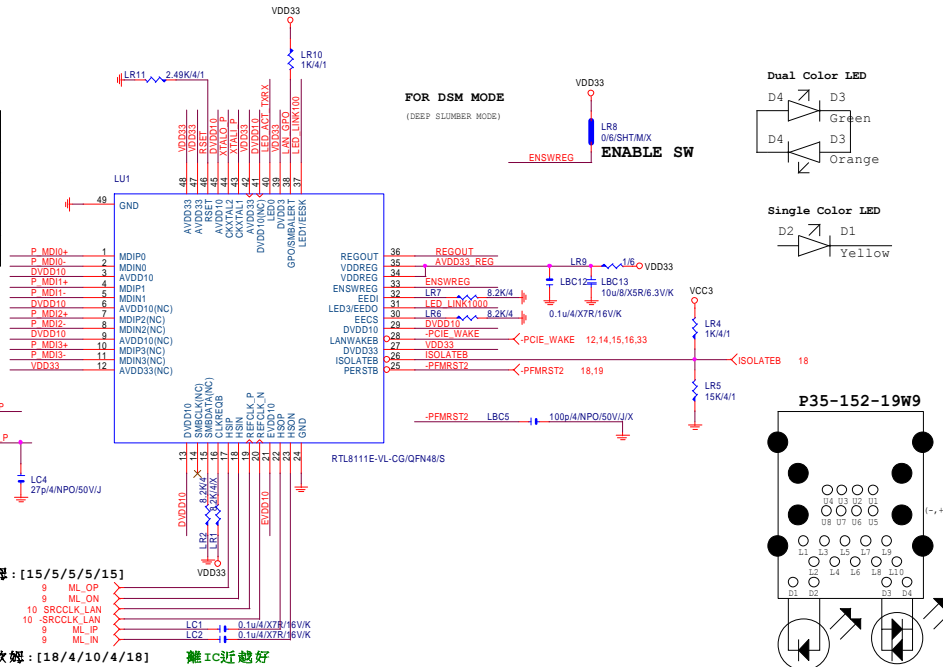
Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custm	GA-Z68AP-D3	2.0	
Date:	Monday, September 19, 2011	Sheet	31 of 35

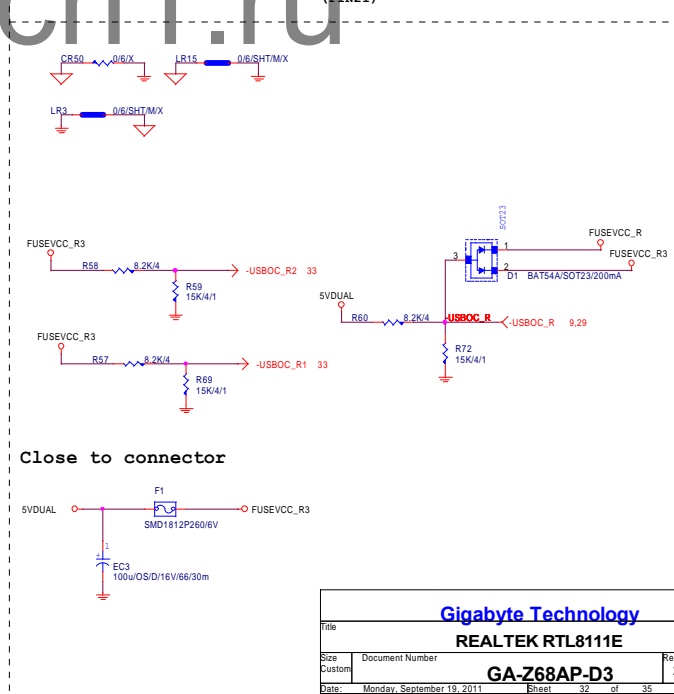
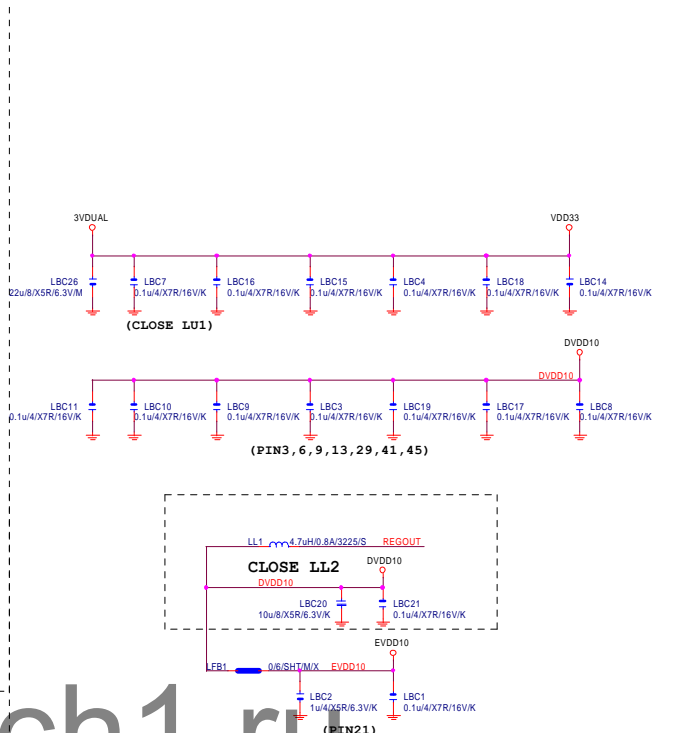
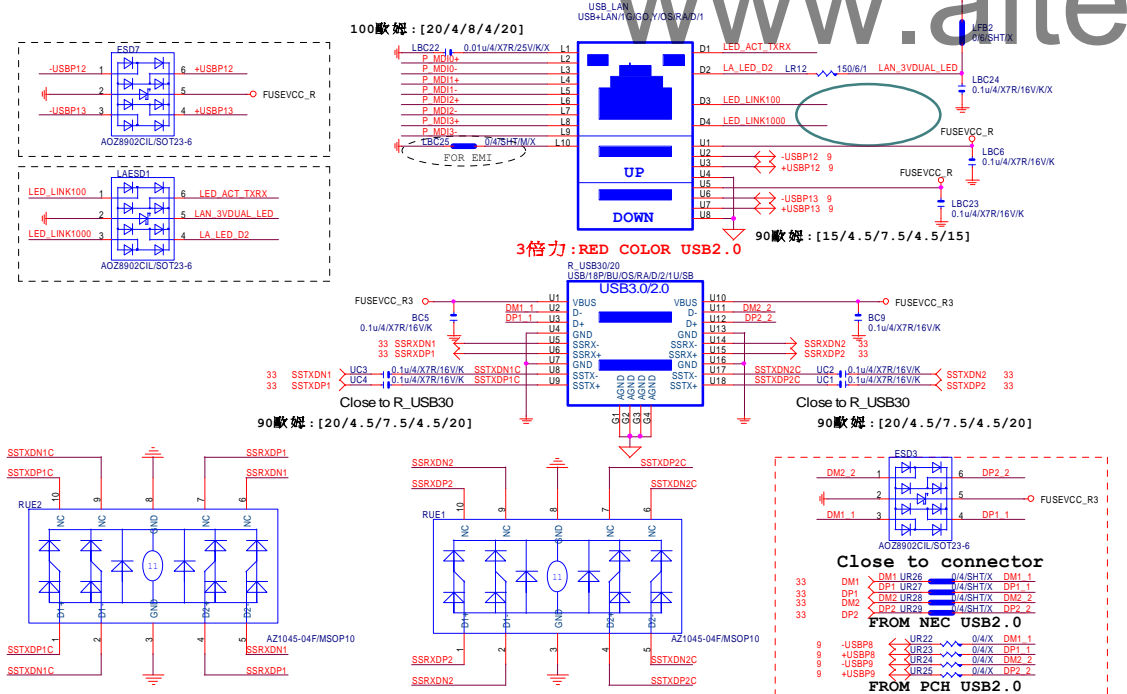
PCIE-1G LAN

Power domain chart

AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB30 LAN CONNECTOR

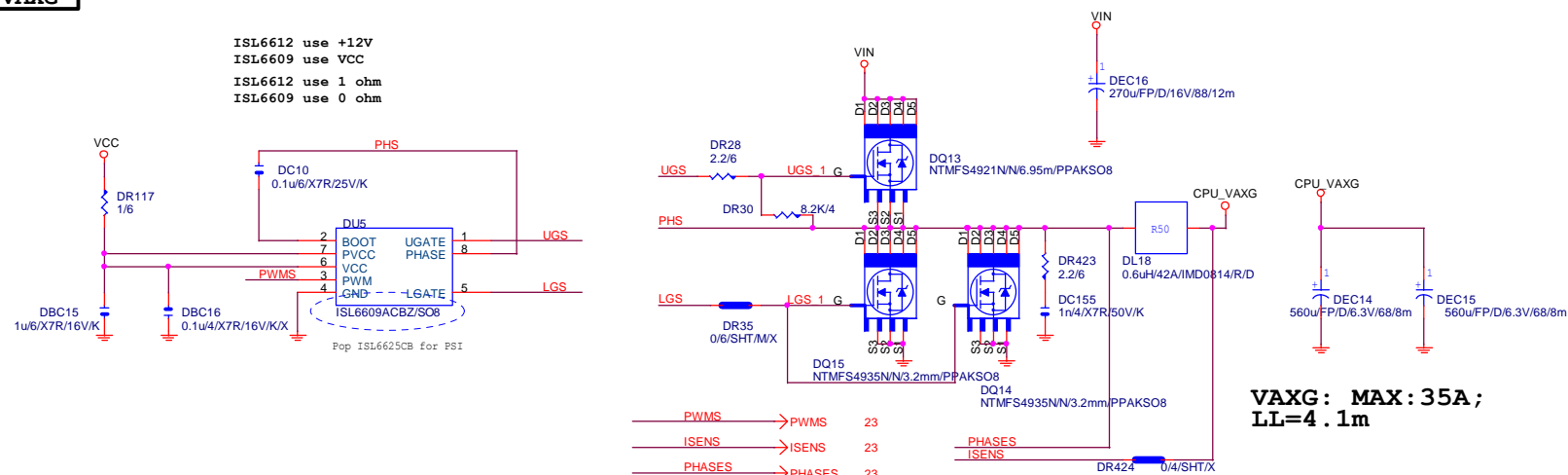


Gigabyte Technology			
REALTEK RTL8111E			
GA-Z68AP-D3			
File	Document Number	Rev	2.0
Size	Custom	Monday, September 19, 2011	Sheet 32 of 35

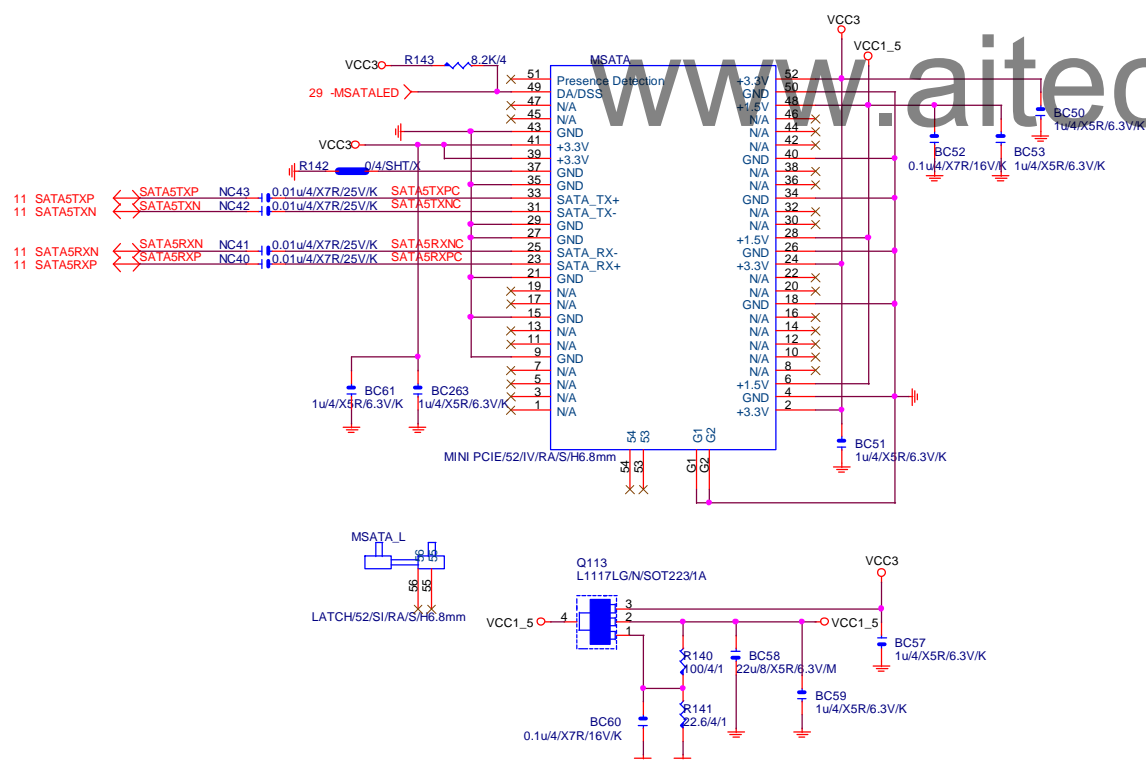
VAXG

```
ISL6612 use +12V
ISL6609 use VCC

ISL6612 use 1 ohm
ISL6609 use 0 ohm
```



VAXG: MAX:35A;
LL=4.1m



GIGABYTE™

Title
VAXG PHASE

Size	Document Number
Custom	GA-Z68AP-D3

Rev	2.0
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